Direct evidence for grain-boundary depletion in polycrystalline CdTe from nanoscale-resolved measurements

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We use scanning probe microscopy-based methods for direct characterization of a single grain boundary and a single grain surface in solar cell-quality CdTe, deposited by closed-space vapor transport. We find that scanning capacitance microscopy can serve to study polycrystalline electronic materials, notwithstanding the strong topographical variations. In this way, we find a barrier for hole transport across grain boundaries, a conclusion supported by the much more topography-sensitive scanning kelvin probe microscopy, with some variation in barrier height between different boundaries. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1542926]

Several types of thin film polycrystalline (PX) solar cells significantly outperform their single-crystal analog.[1] This is surprising as grain boundaries (GBs) are known as two-dimensional defects, and in PX cells the electronic carriers need to cross GBs during transport. Crystal defects and impurities in the GBs can cause formation of localized energy states in the band gap. These can capture carriers from the bulk material, creating localized charge. To neutralize that charge, depleted space charge regions will form near the GB, causing band bending and a barrier for transport of majority carriers.[2] GBs can also decrease the photocurrent by enhanced recombination of photogenerated carriers via GB in-gap states.[2] At the same time, GB band bending may help spatial separation of photogenerated electron-hole pairs and facilitate channeling of carriers along the GBs.[2] Proper analysis of the cell's performance is thus contingent upon thorough understanding of the electronic properties of GBs. Unfortunately, it is very hard to experimentally separate GB from bulk effects. This information is commonly deduced by fitting macroscopic measurements to computational models, which average over different GB length and directions (cf. Refs. 3–5).

GBs in CdTe are of particular interest, as thin film *p*-CdTe/*n*-CdS solar cells (Fig. 1, inset) show great promise for application in large area, low cost photovoltaic systems.[6] Measurements of electrical properties of a single GB in CdTe have been reported using bicrystals,[7,8] even though these are unlikely to represent the GBs of a PX film in a solar cell. Such films undergo heat treatments and consecutive deposition of other layers, as part of the solar cell manufacture, resulting in modified GB chemistry and properties. Attempts at single grain/GB characterization were made with electron beam induced current (EBIC).[9] However, use of EBIC is problematic, as its resolution is limited by the carrier diffusion length,[10] which is in the order of the grain size in low-doped (compensated) *p*-CdTe (0.15–3.1 μm).[11] Here we report direct characterization of single GBs and grain surface properties in solar cell-quality CdTe. This is made possible by judicious use of scanning capacitance microscopy (SCM), supported by scanning kelvin probe microscopy (SKPM), which allow high-resolution, spatial mapping of surface potentials and carrier concentrations close to the sample surface.

Cell structures (without contact to CdTe) were provided by Ferekides (Univ. S. Florida). They were fabricated on 7059 glass, coated with 800–1000 nm transparent conductive oxide of SnO_2:F. PX *n*-CdS (80–100 nm thick) was deposited on the SnO_2 by chemical bath deposition, followed by closed space vapor transport of the PX *p*-CdTe layer (3–7 μm thick) and $CdCl_2$-vapor treatment at 400 °C. The samples were sonicated in de-ionized water (10 min) to remove residual $CdCl_2$, then etched with 0.1% v/v Br_2/methanol for 10–20 s to remove the surface oxide, washed in methanol, and dried in a N_2 stream. For SCM measurements the CdTe surface oxide was then regrown by storage in room ambient for 48 h.

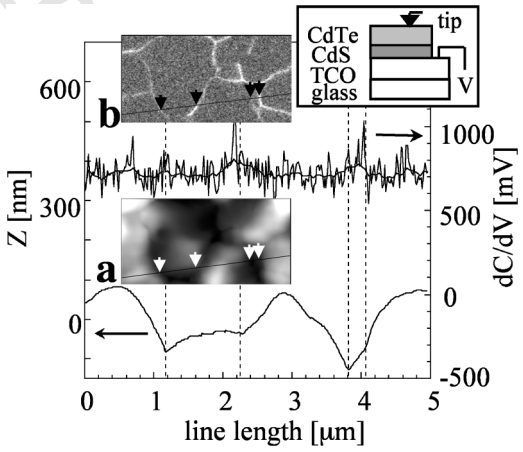

FIG. 1. AFM topography image and line scan (a) and SCM image and line scan (b) of CdTe surface, taken simultaneously. Line scans were taken at the locations indicated by lines in the images. The arrows in the images indicate the locations of GBs, indicated by dashed lines in the graph. The SCM line scan [in (b)] shows both the raw data and the smoothed line, made by application of the Stineman function to the data, with a geometric weight applied to the current point and ±10% of the data range, to arrive at the smoothed curve. The SCM amplitude is given in millivolts, the lock-in amplifier output. Scan size is 2.5 μm×5 μm, using a Pt-coated Si tip (Micromasch). ac bias amplitude used was 2 V at 90 kHz; dc bias applied to the sample was −2 V. The inset (top right corner) shows the schematic arrangement of the measurement.

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In SCM an atomic force microscope (AFM) tip with conductive coating is used to scan the surface in contact mode. The tip and sample surface, with an oxide layer on the surface, form a metal–insulator–semiconductor structure. Simultaneously with the topography data collection, ac bias is applied to the sample while the tip is grounded. The capacitance change, caused by the ac bias (dC/dV), is measured by a high sensitivity capacitance sensing circuit, using a lock-in amplifier. The measured capacitance is the series capacitance of that of the insulator and the semiconductor surface space charge layer. As the sample voltage becomes more negative relative to the tip, the width of the surface depletion layer in *p*-type semiconductor will increase; hence, the total capacitance will decrease. When the sample voltage is positive accumulation will occur and the capacitance measured will be that of the oxide layer only. For *n*-type samples the effects are opposite, which means that the sign of the measured dC/dV signal changes between *n* and *p* type. The magnitude of the change in the depletion layer width for a given dV depends on the carrier concentration. Thus the sign of the dC/dV signal indicates the doping type and the magnitude correlates with the semiconductor's carrier concentration.[12] SCM was done with a Digital Instruments Dimension 3000. The system parameters were arranged so that *p*-type samples show a positive (brighter than a reference) signal, with a brighter signal indicating a higher dC/dV value (*vice versa* for *n* type). For *p*-CdTe with sample bias of 1 V (see later), brighter signals indicate lower hole concentration, as deduced from independent reference measurements. The samples were biased via the transparent conductive oxide.

The PX nature and the fact that the samples contain a diode junction posed problems that needed to be solved to assure meaningful measurements: (1) Surface roughness may affect SCM measurements through changes in the tip-surface contact area. Comparing line scans (Fig. 1) suggest that the SCM line does not follow the topography contour. In addition, measurements at different V_{dc} can show a reversed GB-surface SCM contrast, ruling out topography effects. (2) As we are interested in (near) surface effects we need to avoid measuring the SCM signal related to the cell's junction. Therefore, measurements were taken with the junction under forward bias (-1 V), where it behaves as a conductor and does not contribute to the measured capacitance.

Topography and SCM images of the CdTe surface, following etching in Br_2/methanol and growth of oxide, are shown in Fig. 1. Brighter dC/dV signals are seen at the GBs, compared to the grain surface, as is also evident from comparing line sections of the topography and SCM signal of the same scanned line. This corresponds to a lower hole concentration in the vicinity of the GBs. The SCM line scan [Fig. 1(b)] shows that this hole depletion width changes from one GB to another, and extends 100–300 nm on each side of the GB. Even though the raw line scans are noisy, both the smoothed line scans [see caption of Fig. 1(b) for smoothing procedure], and estimates from SCM images [cf. Fig. 1(b)], confirm this range. These widths are of the same order of magnitude as the Debye length (150 nm) in CdTe with bulk doping density of 7×10^{14} cm^{-3}.[4] Our observations are consistent with models explaining macroscopic transport measurements, suggesting depletion near the GBs as a result of interface states acting as hole traps.[3,4,7]

The differences in dC/dV between GB and grain surface vary from GB to GB (although the GB dC/dV is always higher than the grain surface one), indicating differences in the hole concentration near different GBs. As the concentration and energy distribution of these interface states depend on the GB chemistry and the mismatch between the CdTe crystallographic planes, variations in behavior between different GBs is reasonable.[13]

In addition to GB depletion, increased doping concentrations, adjacent to GB depletion in PX–CdTe, have been suggested from macroscopic measurements.[4,9] The resulting band bending should then enhance separation of electron-hole pairs and channeling along GBs. Indeed, occasional enhanced collection efficiency of photocurrent along GB has been reported, using near-field scanning optical microscopy of a cell cross section with excitation energies close to the CdTe band gap.[14] However, we did not find evidence for an accumulation region adjacent to the depletion region near the GB. Still, we cannot exclude the possibility that the width of this accumulation layer is below the resolution limit of SCM (estimated to be 50 nm for these measurements).

To corroborate our findings we measured SKPM on these samples. SKPM is a noncontact AFM method, where a conductive tip serves as a kelvin probe to measure the surface potential. An oscillating voltage with amplitude V_{ac} is applied to the tip, creating an oscillating force on the tip cantilever, at the same frequency, with amplitude $F=(dC/dZ)V_{dc}V_{ac}$; dC/dZ is the vertical derivative of the tip/sample capacitance, V_{dc} is the dc voltage difference between the tip and the sample. When the tip and the sample surface are at the same potential ($V_{dc}=0$), the cantilever feels no oscillating force. The potential applied to the tip is then equal to the local contact potential difference (the difference between tip and sample work functions). The tip potential is plotted as a function of tip position, creating a surface potential map.[15,16] In a semiconductor sample the effective work function is the sum of the ''theoretical'' work function, derived from the bulk properties, and the surface band bending and dipoles. SKPM measurements were performed in air using a P47 Solver Scanning Probe microscope (manufactured by NT-MDT, Russia). The samples were grounded via the transparent conductive oxide.

Electrostatic forces are long range. Therefore, the forces acting on the tip are not only due to the local interaction but arise also from distant locations. Thus, the rough CdTe surface topography (height differences up to ~0.5 μm) may introduce features in the SKPM image which are due to convolution of topographic and electronic data. To minimize topography effects, each line was scanned first in noncontact AFM mode. A second scan followed the topography contour at a constant tip-sample separation, with ac modulation at the cantilever resonance frequency and a different feedback circuit to monitor the SKPM signal. No mechanical polishing was used for surface flattening, so as not to introduce additional surface defects.

SKPM mapping of the CdTe backsurface shows images that follow the topography features closely, especially near the GBs, as is also evident from line scans (Fig. 2). The GBs

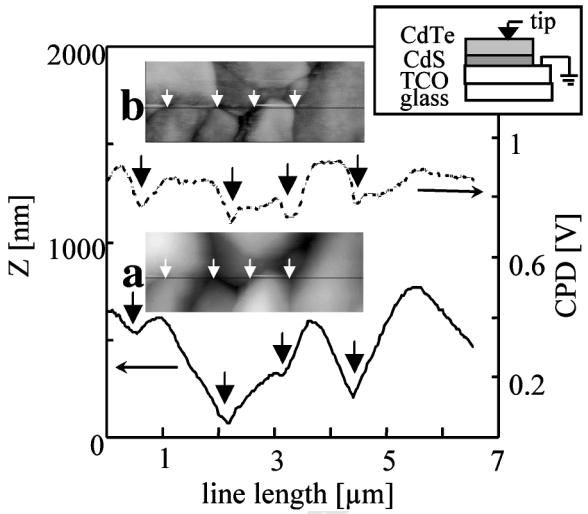

FIG. 2. AFM topography image and line scan (a), and SKPM image and line scan (b) of CdTe surface, taken simultaneously. The lines in the images indicate the locations of the line scans. The arrows indicate the locations of GBs. Scan size was 2.4 μm$\times$6.7 μm, using a TiO_{2-x}-coated Si tip (Micromasch). The tip-sample separation was 30 nm, and the ac voltage amplitude was ~6 V. The inset (top right corner) shows the schematic arrangement of the measurement.

show lower SKPM values (darker contrast) than the outer CdTe grain surface. Based on our SCM measurements, we can conclude that this is not just an artifact related to convolution with topography, but is related to lower hole density near the GB, which reduces the local work function. Sadewasser *et al.* suggested a similar argument for PX–$CuGaSe_2$ and $Cu(In,Ga)S_2$ in thin-film solar cells, based solely on SKPM.[17] Quantitative measurements of the band bending at the GBs were not possible, as the topography-related effect is superimposed on the work function-related signal.

Since closed space vapor transport-deposited CdTe grains are not columnar but rather isotropic in shape, the photocurrent is expected to cross at least 1–2 GB barriers between the backsurface and the CdTe/CdS junction. As the AFM feedback laser (670 nm) illuminates the sample during measurements, the GB barriers appear to be non-negligible under illumination and, thus, should be present also under solar cell operating conditions. The relatively high efficiency displayed by such cells then suggests that these GB barriers do not affect cell operation significantly. Hence, the cause for the superiority of PX over single crystalline devices must be sought elsewhere, possibly the earlier-mentioned improved photocurrent collection along GBs.[14]

To conclude, we have shown that SCM can serve to study PX electronic materials, notwithstanding their strong topographical variations. We directly observe the presence of a barrier for hole transport across GBs in solar-cell quality CdTe, a conclusion supported by SKPM data. The barrier height varies between different GBs. This barrier is expected to affect intergrain hole transport of the photocurrent. The demonstrated superiority of PX over single crystalline CdTe/CdS cells therefore implies that other mechanisms of current collection are operative in these cells.

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